

## CLAIMS:

1. A parallel data processing device comprising:  
an array of parallel processing elements (LPA1...320) for processing a signal to  
obtain parallel streams of data, and  
means (TSMM1...80) for shuffling the parallel streams of data in a block-wise  
5 manner.

2. A device as claimed in claim 1,  
wherein the data shuffling means (TSMM1...80) comprise an array of  
addressable switch memory matrices (TSMM1...80) which are each coupled to a  
predetermined number of processing elements (LPA1...320).  
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3. A device as claimed in claim 2, wherein each switch memory matrix  
(TSMM1...80) comprises:  
a matrix of registers (MR); and  
15 a crossbar switch having row-wise buses (r1...4) and column-wise buses  
(c1...4), crossings of the row-wise buses (r1...4) and the column-wise buses (c1...4) being  
provided with switches (T), each register (MR) being coupled to one row-wise bus (r1...4) and  
one column-wise bus (c1...4) of the crossbar switch, and each column-wise bus (c1...4) being  
coupled to a processing element (LPA1...320).  
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4. A device as claimed in claim 2,  
wherein each switch memory matrix (TSMM1...80) is a square matrix.

5. A device as claimed in claim 2,  
25 wherein the switch memory matrices (TSMM1...80) are coupled two by two to  
each other.

6. A device as claimed in claim 2,

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5 7. Camera system comprising:  
a sensor array (S) for obtaining a signal; and  
a parallel data processing device as claimed in claim 1 for processing the signal.

8. A camera system as claimed in claim 7,  
10 wherein the sensor array (S) is provided with a color filter array, and a number  
of columns of the sensor array (S) corresponding to different colors (R,G,B) are shared by a  
same processing element (LPA1...320).

9. A method of processing a signal, comprising the steps of:  
15 processing the signal in an array of processing elements (LPA1...320) to obtain  
parallel streams of data, and  
shuffling (TSMM1...80) the streams of data in a block-wise manner.